CDM Simulation Based on Tester, Package and Full Integrated Circuit Modeling: Case Study

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(Invited Paper)

Abstract—The electrostatic discharge (ESD) sensitivity of ICs with respect to the charged-device model (CDM) is strongly dependent on the IC package, the substrate resistivity, and the effectiveness of the ESD protection network. This paper presents a case study of predictive CDM circuit simulation method based on the tester, package, and full IC modeling approach.

Index Terms—Bipolar and complementary metal oxide semiconductor (BiCMOS) integrated circuits (ICs), electrostatic discharge (ESD), SPICE simulations.

I. INTRODUCTION

AMONG THE electrostatic discharge (ESD) test standards, charged-device model (CDM) testing is the one that leads to the most complex failure mechanisms due to the single pin discharge. During a CDM test, the charge stored in the packaged chip by means of the charge plate previously raised up to a predefined potential is discharged to the ground plate through the pin under test (PUT) and the ground pogo pin. The charge flows through the lowest ohmic path to the PUT and then to the grounded plate.

For better understanding of the CDM current distribution and for predicting the voltage drop across some CDM sensitive circuit topologies such as cross-domain devices, the development of simple and accurate models for CDM simulation is very important [1], [2]. This allows improving the predictive capability with respect to the CDM qualification of ICs so that supply clamps, as well as CDM clamps, can be designed and placed accordingly in the chip in order to reduce reliability issues of ICs due to the CDM. A study has shown the effect of the substrate resistivity on the CDM robustness of modern ICs [3].

In this paper, we present a novel approach of a full IC modeling under CDM. The CDM tester and package parasitics are extracted using the time-domain reflectometry (TDR) technique [4]. The substrate current distribution is modeled by the means of a high-frequency electromagnetic simulation tool used for RC-network extraction purposes. A 0.25-μm BiCMOS digital tuner is used as a test case for the predictive CDM simulation of a real CDM cross-domain issue.

This paper has been expanded and enhanced with very fast transmission-line pulse (vf-TLP) analysis of gate-oxide breakdown-voltage test structures of inverter circuits in the CDM time domain. This vf-TLP characterization has given a new insight to the observed CDM failure mechanism in the test case.

Furthermore, additional CDM simulations have been performed to see the influence of bond wires to the CDM cross-domain voltages.

A very good correlation between simulated and measured CDM waveforms was obtained. In addition, a good correlation was found between the predicted failure and the actual CDM failures that occurred in the test case.

II. CDM TESTER MODEL VALIDATION

All CDM qualification results and discharge waveforms of products and calibration modules described in this paper were obtained using a Thermo Fischer RCDM3 CDM tester. The CDM tester parasitics were characterized and extracted, following the traceable method described in [5].

In order to validate and improve the model of the CDM tester, CDM discharge waveforms have been simulated and compared with actual measured CDM waveforms from the verification modules. SPICE-based simulations have been performed, based on actual values of the Electrostatic Discharge Association (ESDA) small and large modules. Fig. 1 shows the SPICE model used for the simulation of a CDM discharge on a package pin. In order to calibrate the simulation test bench, the PUT is replaced by the measured value of the calibration targets that are used for calibrating the CDM tester setup, i.e., $C_{\text{SMALL-MODULE}} = 4.6$ pF and $C_{\text{LARGE-MODULE}} = 33.3$ pF for ESDA small and large verification modules, respectively.

The oscilloscope is represented by the $R_{\text{SCOPE}} = 50$ Ω input resistor and a 6-GHz Butterworth filter. Furthermore, $R_{\text{CHARGE}} = 100$ MΩ, and $R_{\text{PROBE}} = 1$ Ω.

Very good agreement is achieved between simulations and measurements, except for the third peak of the large ESDA module (see Fig. 2). This is not considered to be relevant because of the low current and the fact that real package capacitance values are significantly lower than the ESDA large module.

The R_{ARC} is the impedance of the electrical arc; it represents the resistance of the air-discharge process at the discharge pin during CDM, which is used as a fitting parameter for the CDM
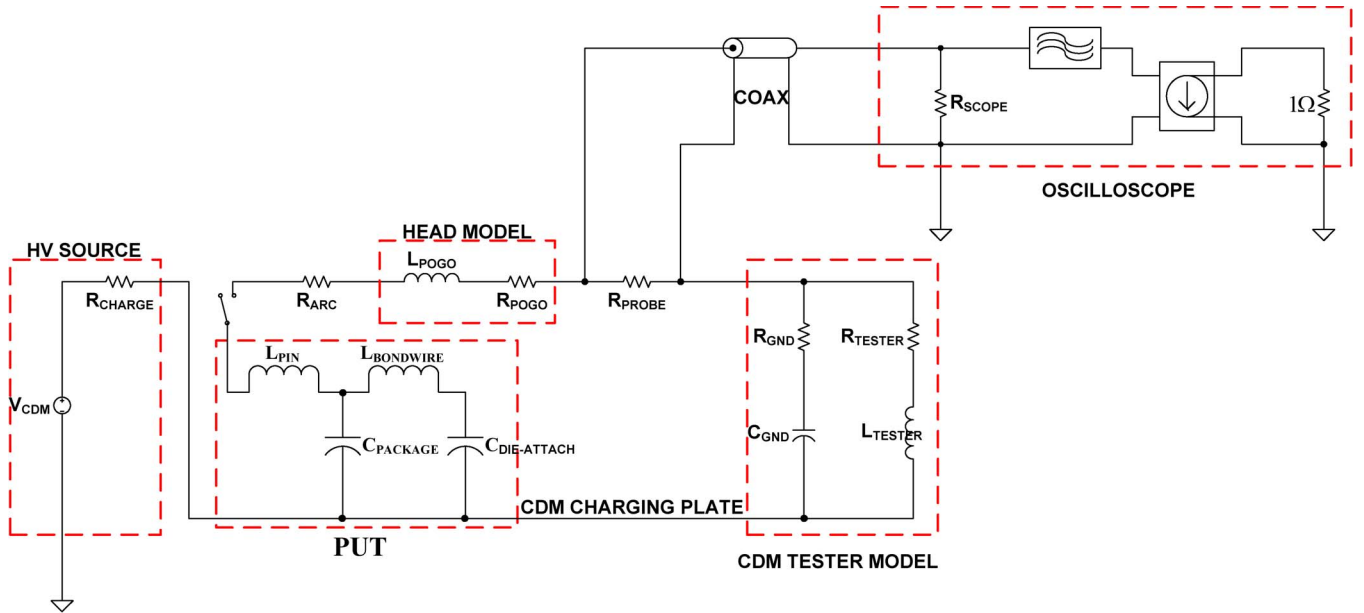
Fig. 1. SPICE model of the CDM discharge setup including the CDM tester and PUT parasitics.
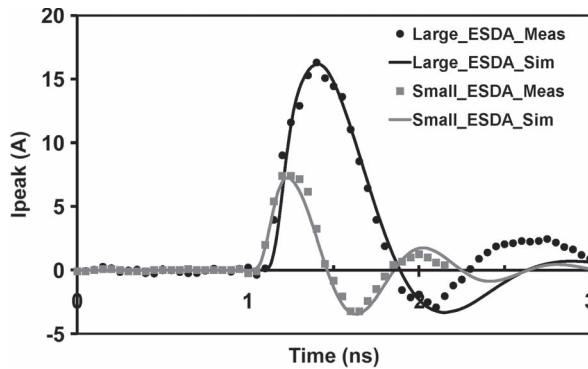

Fig. 2. 500-V (positive) CDM discharge current of the small and large ESDA modules (simulated $R_{\mathrm{ARC}} = 33\ \Omega$).

TABLE I
TESTER PARAMETERS FOR THE ESDA CONFIGURATION EXTRACTED
USING THE METHOD DESCRIBED IN [5]

Tester Parameters	ESDA
L_{POGO}	2.3nH
R_{POGO}	200mΩ
$R_{\mathrm{GROUND\ PLANE}}$	25Ω
$C_{\mathrm{GROUND\ PLANE}}$	25pF
L_{TESTER}	3μH
R_{TESTTER}	1Ω

peak current. The simulated value of the impedance of the electrical arc R_{ARC} is in the range of 30 Ω and is in line with other published studies [6].

Table I summarizes the main settings used in the calibration waveform verification and the CDM tester parasitics.

III. IC PACKAGE LUMPED-ELEMENT MODEL

A. Parasitics Extraction Using TDR

The impedance profile of various pins of selected design has been characterized for modeling purposes. This includes different packages, different bond wire lengths, and different die sizes. We have used the following TDR setup:

1) Agilent 86100A Infinium DCA wide bandwidth oscilloscope with 18 GHz sampling bandwidth;
2) Agilent 54754A Differential TDR module with a rise time of 40 ps;
3) Tektronix P8018 Handheld TDR probe with a bandwidth of 20 GHz and characteristic impedance of 50 Ω;
4) DVT30-1MM GigaProbes TDR/TDT with bandwidth of 30 GHz and differential input impedance of 100 Ω.

TDR uses a technique that is comparable to radar: the TDR instrument sends a fast electrical pulse through the PUT and monitors the time to receive reflections. These reflections can correspond to capacitive, inductive, or resistive distortion of the PUT impedance. The resulting waveform is the combination of the incident step and reflections generated when the step encounters impedance deviations from 50 Ω [7].

An inductive discontinuity will be visible on a TDR waveform as a spike above the impedance of the surrounding transmission lines, whereas a capacitive discontinuity will be visible as a dip in the impedance profile waveform. The corresponding values for inductance and capacitance can be computed as described in [4].

B. Validation of the IC Package CDM Model

The parasitic extraction method described in the previous section has been applied to Low profile Quad Flat Pack (LQFP), Heatsink Very-thin Quad Flat-pack No-leads (HVQFN), and Flip Chip Ball Grid Array (FCBGA) packages (see Table II). The average equivalent package capacitance C_{PACKAGE} of the PUT varies from 2 to about 8 pF for LQFP80 and FCBGA806, respectively. Furthermore, the value of the self-inductance L_{BONDWIRE} of the bonding wire increases with length.

The extracted lumped circuit is integrated into the model defined in Fig. 1 and used to simulate the CDM discharge and

TABLE II
AVERAGE LUMPED-ELEMENT PARAMETERS OF A TYPICAL PUT
EXTRACTED FROM TDR MEASUREMENTS OF IC PACKAGES

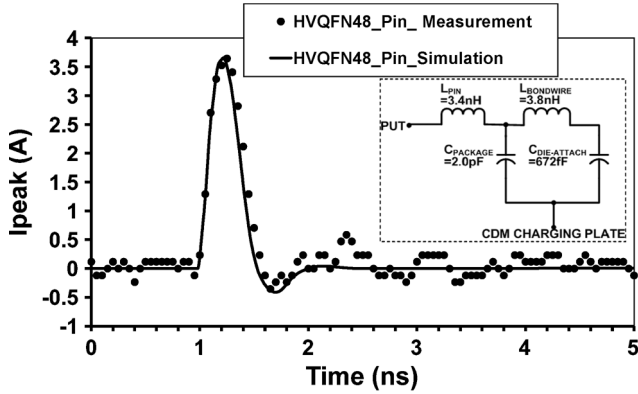| Package	L_{PIN}	$C_{PACKAGE}$	$L_{BONDWIRE}$	$C_{DIE\text{-}ATTACH}$
HVQFN48	3.4nH	2.0pF	3.8nH	0.67pF
LQFP80	6.6nH	1.9pF	5.7nH	0.62pF
FCBGA806	3.2nH	8.2pF	18.9nH	2.0pF

Fig. 3. Simulated versus measured 500-V CDM discharge waveforms of the test case product PUT (simulated $R_{ARC} = 30\ \Omega$). The equivalent lumped circuit of the PUT is shown in the inset.

to compare with actual CDM discharge waveforms measured from these IC packages.

Good agreement is shown in Fig. 3 for the HVQFN48 package of the BiCMOS IC. The shape of the discharge current waveform depends on package properties. The model is able to reproduce this very well.

IV. FULL IC MODELING

A. ESD Protection Network Modeling

The ESD protection network of the product studied in Section VI is a rail-based ESD protection scheme using diodes and a Darlington bipolar "the crowbar" as active main supply clamps [8]. All the neighboring ground domains of the IC are coupled to each other with antiparallel diodes in the I/O ring. The equivalent SPICE model of the ESD protection network has been extracted by means of a vf-TLP measurement. The RC-trigger crowbar, as well as the ESD diode, can be simulated using SPICE models directly, as shown in the inset in Fig. 4.

Furthermore, in order to take into account the effective resistance due to the supply and ground metal buses from the ESD protection network, a systematic pad-ring layout checking method has been developed. Using the script, we can detect the I/O with the highest equivalent resistance to the clamp for each power domain. Fig. 5 shows that the worst case for the effective ground bus resistance is for both the VSS1 and VSS4 domains. (VSS1 = 0.55 Ω and VSS4 = 0.74 Ω.)

B. Full Chip Substrate Modeling

In order to model the substrate of a chip with N ground domains in the CDM timeframe, an N-port S-parameter simulation is performed on the layout of the chip with Ansoft's 3-D
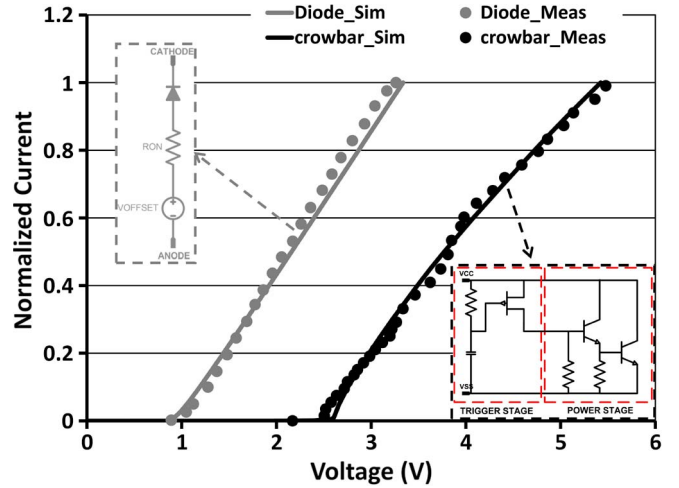

Fig. 4. SPICE simulations versus vf-TLP testing of the ESD diode and the RC-trigger crowbar. Equivalent models of the diode and the crowbar are shown in the inset.
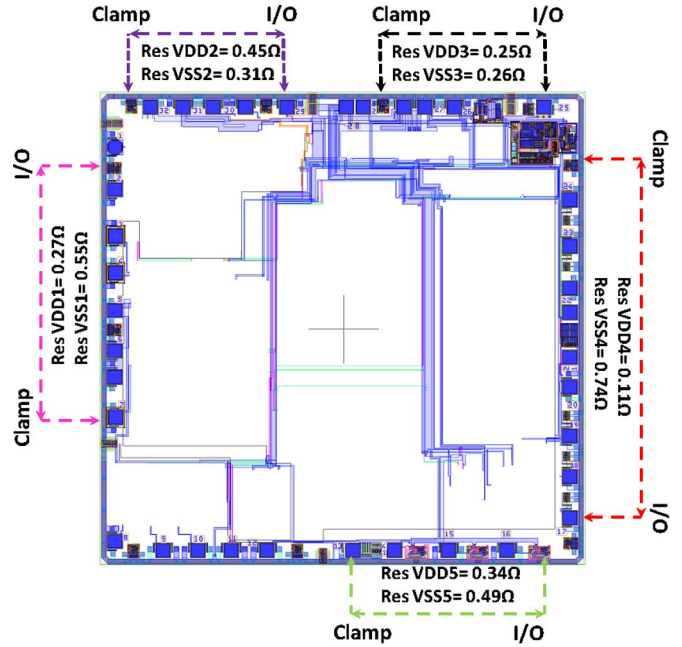

Fig. 5. The I/O pad ring of the BiCMOS IC. The effective resistance of the supply and ground buses for each domain is shown.

full-wave electromagnetic field software (HFSS). For the electromagnetic simulations, 50-Ω-characteristic-impedance lumped ports are used [9].

An equivalent RC network is extracted from all ground domains at the 1.1–2 GHz frequency sweep (corresponding to the frequency spectrum of the CDM discharge at −6 dB) [10].

This RC network is extracted from the simulated N by N admittance (Y-parameters) matrix using (1)–(4), as follows:

$$[Y] = \begin{Bmatrix} Y_{11} & \cdots & Y_{1j} & \cdots & Y_{1N} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ Y_{i1} & \cdots & Y_{ij} & \cdots & Y_{iN} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ Y_{N1} & \cdots & Y_{Nj} & \cdots & Y_{NN} \end{Bmatrix} \quad (1)$$
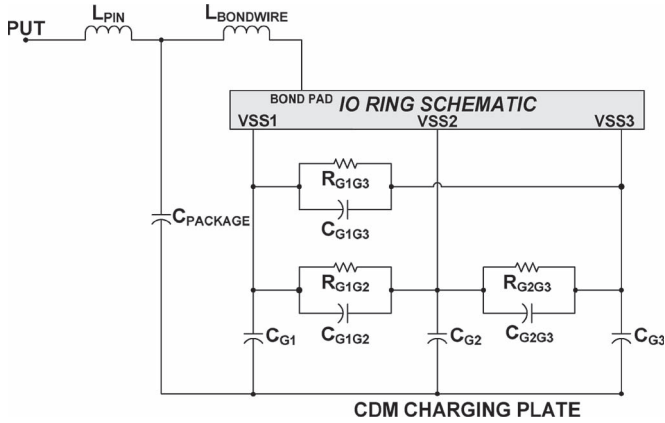
Fig. 6. Example of an RC network extracted from a three-ground-domain chip.

$$Y_{\mathrm{GiGj}} = -(Y_{\mathrm{ij}} + Y_{ji})/2 \tag{2}$$

$$R_{\mathrm{GiGj}} = \mathrm{real}(1/Y_{\mathrm{GiGj}}) \tag{3}$$

$$C_{\mathrm{GiGj}} = \frac{-1}{2 \cdot \pi \cdot f \cdot \mathrm{imag}(1/Y_{\mathrm{GiGj}})} \tag{4}$$

where $i = 1, \ldots, N$ and $j = 1, \ldots, N$, and $f = 1.1$ GHz is the electromagnetic simulation frequency.

R_{GiGj} and C_{GiGj} are the RC parasitics between the two ground domains Gi and Gj and are extracted from Y_{ij}-parameters with $i \neq j$ only. In HFSS, the S-parameters are computed by the finite-element method and are therefore subject to discretization error. A previous work has shown that the computational error of S-parameters is about 2% for $N = 10$ and for about 30 000 tetrahedral meshes [11]. For this paper, the convergence criterion (maximum magnitude delta) of the S-parameters was set to 1% with 43 657 tetrahedral meshes.

The value of the die-attach capacitance $C_{\mathrm{DIE-ATTACH}}$ is distributed over the N-ground nodes of the chip. The value of the capacitance C_{Gi} between the charging plate and each ground domain node is proportional to its die area. In addition, the RC network of the substrate extracted from HFSS simulations and the ESD protection network model are integrated in the CDM simulation test bench, as shown in Fig. 6.

The lumped circuit extracted by the TDR approach from a PUT of the HVQFN48 package (see Table II) of the test case IC is integrated into the model defined in Fig. 1. The capacitance $C_{\mathrm{DIE-ATTACH}} = 672$ fF is distributed between the five ground nodes of the chip, as described earlier. The value of the capacitance C_{Gi} between the charging plate and each ground node is proportional to the die area of the test case chip occupied by the latter. Table III lists the capacitance values per domain, and Fig. 7 shows both the area distribution and the RF current density of the ground domains.

Ten combinations are sufficient to model the RC network of the substrate of the 3.5 mm $\times$ 3.3 mm-digital tuner chip with the substrate resistivity of $\rho = 200 \, \Omega \cdot$ cm. The electromagnetic simulations were performed on a simplified layout to limit the run time and the memory usage. This is done using a shell script that replaces clusters of more than 32 equidistant substrate contacts in one large "super" contact. The substrate parasitic

TABLE III
EQUIVALENT CAPACITANCE BETWEEN THE CDM TESTER CHARGING PLATE AND EACH GROUND DOMAIN OF THE TEST CASE IC

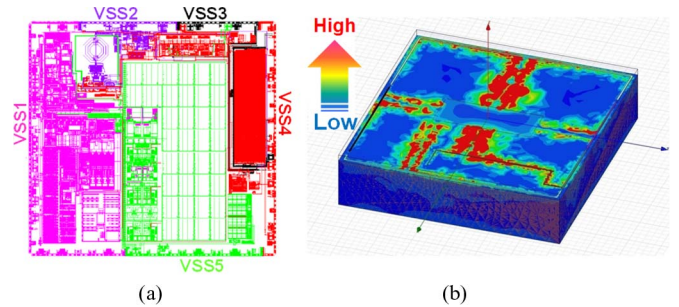| Ground domain	Area	Value [fF]
VSS1	33%	$C_{\mathrm{G1}} = 223.8$
VSS2	8.4%	$C_{\mathrm{G2}} = 56.1$
VSS3	3.6%	$C_{\mathrm{G3}} = 24.5$
VSS4	19%	$C_{\mathrm{G4}} = 126.9$
VSS5	36%	$C_{\mathrm{G5}} = 240.7$
Die	100%	$C_{\mathrm{DIE-ATTACH}} = 672.0$

Fig. 7. (a) On-chip ground domains of the test case IC layout showing the area distribution of each ground domain across the chip (b) and the 3-D view of the RF current density of the substrate ground domains in HFSS.

TABLE IV
SUBSTRATE PARASITIC RESISTANCE AND CAPACITANCE EXTRACTED FROM THE FIVE GROUND DOMAINS OF THE TEST CASE IC. THE SUBSTRATE RESISTIVITY IS $\rho = 200 \, \Omega.$cm

Ground domain	Resistance [kΩ]	Capacitance [fF]
VSS1/VSS2	$R_{\mathrm{G1G2}} = 1.75$	$C_{\mathrm{G1G2}} = 45.8$
VSS1/VSS3	$R_{\mathrm{G1G3}} = 1.05$	$C_{\mathrm{G1G3}} = 68.1$
VSS1/VSS4	$R_{\mathrm{G1G4}} = 1.12$	$C_{\mathrm{G1G4}} = 64.1$
VSS1/VSS5	$R_{\mathrm{G1G5}} = 1.50$	$C_{\mathrm{G1G5}} = 52.5$
VSS2/VSS3	$R_{\mathrm{G2G3}} = 2.19$	$C_{\mathrm{G2G3}} = 37.3$
VSS2/VSS4	$R_{\mathrm{G2G4}} = 3.43$	$C_{\mathrm{G2G4}} = 20.3$
VSS2/VSS5	$R_{\mathrm{G2G5}} = 5.68$	$C_{\mathrm{G2G5}} = 12.1$
VSS3/VSS4	$R_{\mathrm{G3G4}} = 0.76$	$C_{\mathrm{G3G4}} = 119.8$
VSS3/VSS5	$R_{\mathrm{G3G5}} = 2.64$	$C_{\mathrm{G3G5}} = 26.6$
VSS4/VSS5	$R_{\mathrm{G4G5}} = 1.95$	$C_{\mathrm{G4G5}} = 43.0$

RC-network parameters extracted from HFSS simulations of the test case IC are summarized in Table IV.

CDM simulations performed at 500 V showed that only a negligible portion, i.e., few milliamperes, of the CDM current was actually flowing in the substrate (see Fig. 8). Most of the CDM current is flowing into the ESD protection network. Therefore, the inductive contribution of the ground routing has not been taken into account in the modeling of the substrate.

V. VF-TLP ANALYSIS OF THE GATE-OXIDE BREAKDOWN VOLTAGE

A. Test Structure Description

To determine the typical gate-oxide breakdown voltages for this technology in the CDM-like time domain, dedicated test
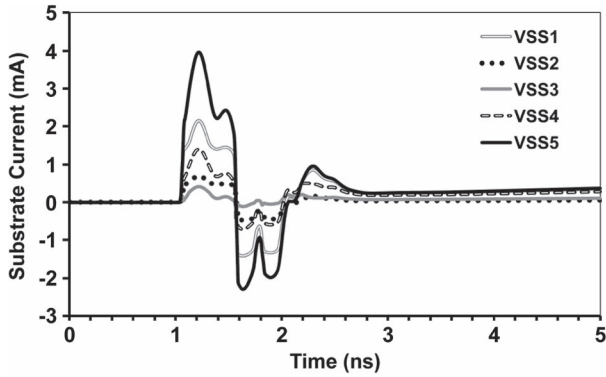
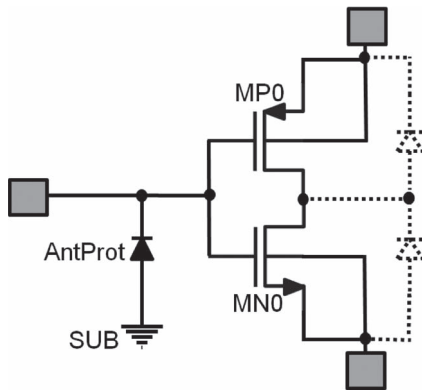Fig. 8. Simulated substrate current during the 500-V CDM discharge in the BiCMOS IC.

Fig. 9. Schematic view of the ESD test structures used for vf-TLP characterization. The parasitic back gate diodes of the inverter are shown.

structures have been designed. These test structures replicate the internal I/O circuit (inverter) of the receiver that belongs to the VDD1/VSS1 domain of the test case BiCMOS IC. MP0 and MN0 are the PMOS and NMOS transistors (PMOST and NMOST, respectively) of the inverter, respectively, with a W/L ratio of $75/0.25$ μm (see Fig. 9). The antenna protection diode connected to the gate of the receiver inverter is placed for manufacturability reasons only and is not intended for CDM protection because of its very small size. Furthermore, this antenna protection diode has been placed in the test structure in order to fully replicate the configuration of the receiver inverter, as for the test case IC described in Section VI.

B. Vf-TLP Results

A calibrated 2.5-ns vf-TLP with 0.3-ns rise time was used for the characterization of the ESD test structures described in the previous section. The gate oxide of both the NMOST and PMOST from the inverter was vf-TLP stressed in inversion and accumulation modes. Fig. 10 shows the gate–source breakdown voltages in both inversion and accumulation modes for the PMOST and the NMOST. The gate-oxide breakdown voltage is stress polarity dependent; the inversion mode is a more severe stress for the NMOST than the accumulation mode. In addition, it is the other way around for the PMOST. These vf-TLP results confirm the same trend as already described in the literature [12] for the 100-ns TLP stress of "thick" gate oxide (i.e., thickness > 2.5 nm).
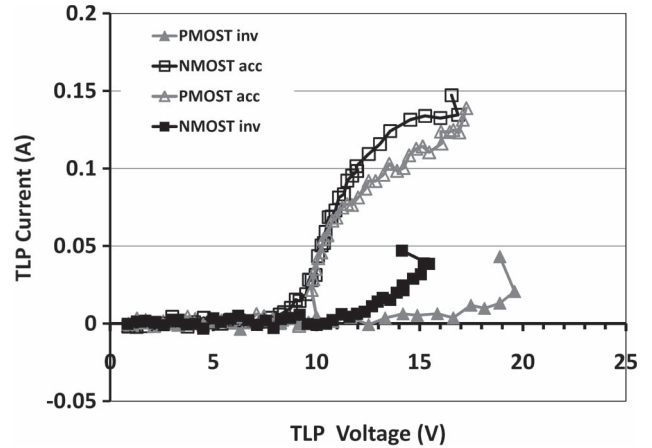

Fig. 10. VF-TLP characterization results of the gate-oxide breakdown voltage, up to gate-oxide failure, of an NMOST and a PMOST in various configurations.

TABLE V
GATE-OXIDE BREAKDOWN VOLTAGES IN THE CDM TIME DOMAIN

Device	Inversion Mode	Accumulation Mode
NMOST	BV_{OX}=15.4V	BV_{OX}= 16.8V
PMOST	BV_{OX}=19.6V	BV_{OX}= 17.2V

Note that, in the accumulation configuration, the antenna protection diode starts conducting ESD current at about 10 V in avalanche mode.

The values of the gate-oxide breakdown voltages of this 5-nm gate-oxide technology in the CDM-like regime are summarized in Table V.

VI. PREDICTIVE CDM SIMULATIONS

In this section, the CDM simulations approach developed in this paper will be demonstrated by the analysis of a CDM fail in a digital tuner IC in a BiCMOS technology. The influence of bond wires to the CDM cross-domain voltages is discussed as well.

Note that, for all the simulated CDM discharge waveforms shown in this section, the CDM-stressed PUT is an I/O that belongs to the VDD4/VSS4 domain of the test case BiCMOS IC.

A. Cross-Domain Voltage Simulations of the BiCMOS IC

The product passed 400-V CDM qualification but failed 500 V (negative). The failure analysis revealed a gate-oxide defect in a cross-domain circuit. The gate of an NMOST receiver from the VDD1/VSS1 domain and driven by a driver from the VDD4/VSS4 is damaged by a large voltage stress due to CDM. No damage was observed on the PMOST (see Fig. 11).

CDM discharge simulations have been performed on the PUT from the VDD4/VSS4 domain in order to monitor the internal I/O node voltage (see the schematic in Fig. 12).

The CDM discharge voltage is simulated at −500 V (see Fig. 13), and the analysis of the simulated cross-domain voltage
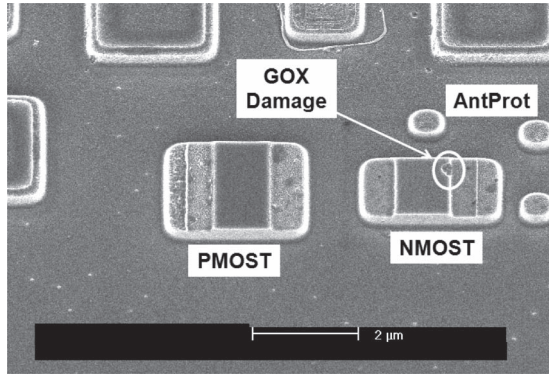
Fig. 11. Gate-oxide defect in an NMOST from a VSS1 receiver due to CDM stress at -500 V. Note that the PMOST is not damaged.
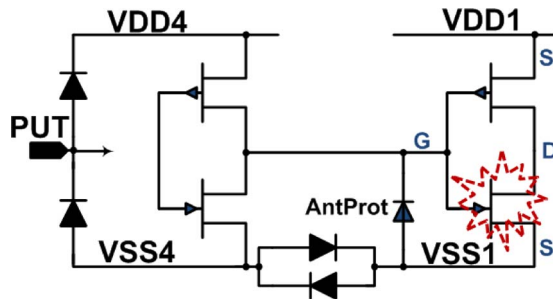

Fig. 12. Schematic of the internal I/O circuit (cross domain), with the driver in VDD4 domain and the receiver in the VDD1 domain. The NMOST that is damaged due to CDM stress is also shown. The ESD protection clamps are not included in this schematic.
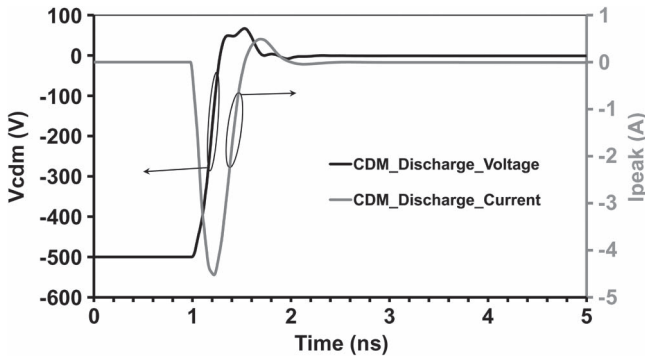

Fig. 13. Simulated CDM voltage and current discharge waveforms of the PUT at -500 V.

waveforms in Fig. 14 shows that, at -500-V CDM, the peak voltage $V_{GS}-$ NMOST across the gate oxide of the receiver NMOST is higher than the measured gate-oxide breakdown voltage of the NMOST in inversion mode ($V_{GS}-$ NMOST $=$ 15.8 V $>$ BV$_{OX}$ = 15.4 V). Interestingly, the peak voltage $V_{GS}-$ PMOST across the gate oxide of the receiver PMOST is lower than the measured gate-oxide breakdown voltage of the PMOST in accumulation mode ($V_{GS}-$ PMOST $=$ 11.5 V $\leq$ BV$_{OX}$ = 17.2 V). These simulations correlate very well with the failure analysis; since only the gate oxide of the receiver NMOST was damaged, no defect was observed on the receiver PMOST at -500-V CDM. Furthermore, these results also confirm that, during negative CDM of the PUT, the receiver
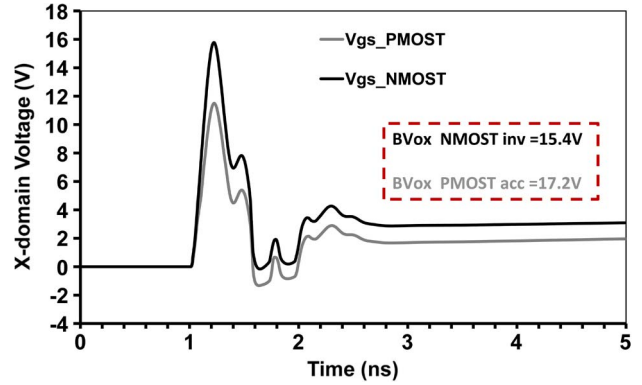

Fig. 14. Simulated cross-domain voltages of the test case IC at -500-V CDM. The gate–source voltage waveforms of the receiver NMOST and PMOST are shown. The doted box in the inset recalls the measured BV$_{OX}$ of the NMOST and the PMOST in the CDM regime for this technology.

NMOST gate is stressed in inversion mode, whereas the receiver PMOST gate is stressed in accumulation mode.

It is also interesting to notice that the simulated peak voltage V_{GS}-NMOST is higher than the peak voltage V_{GS}-PMOST of the receiver. This is due to the direct substrate $R \| C$ coupling between VSS1 and VSS4.

For complete predictive analysis, similar simulations must be done for all cross-domain combinations.

B. Effect of the IC Package Bond Wires on CDM Cross-Domain Voltages

In order to study the impact of the IC package bond wires on the CDM cross-domain voltages, additional CDM simulations were performed using all the test case IC parameters extracted as described in this paper, except the ESD protection network between VSS1 and VSS4. The purpose was to see "what would happen if." The CDM simulations have been performed with the following configurations.

1) CONFIGURATION 1: No antiparallel diodes between VSS1 and VSS4 at chip level but both grounds are connected together with a bond wire equivalent to 2 nH at package level;
2) CONFIGURATION 2: Antiparallel diodes between VSS1 and VSS4 at chip level and both grounds are connected together with a bond wire equivalent to 2 nH at package level;
3) CONFIGURATION 3: No antiparallel diodes between VSS1 and VSS4 at chip level and NO connection at package level between VSS1 and VSS4.

Table VI summarizes the simulated cross-domain voltages for each configuration. The reference is the result of the predictive CDM simulation of the BiCMOS IC.

As expected, the worst case for the cross-domain voltage overshoot is observed when the receiver and the driver ground domains are fully isolated from each other. The voltage overshoot at receiver gate increases by a factor of 36% compared with the reference. Furthermore, these qualitative data from CDM simulations show that, in the case where two different ground domains are bonded out and connected to a common ground at package level, these bond wires will have a beneficial

TABLE VI
SIMULATED CROSS-DOMAIN VOLTAGES WITH DIFFERENT ESD
PROTECTION CONFIGURATIONS BETWEEN VSS1 AND VSS4 DOMAINS

X-domain Voltage	Reference	Config. 1	Config. 2	Config. 3
V_{GS}-NMOST	15.8V	15.3V	14.8V	21.5V
V_{GS}-PMOST	11.5V	11.3V	10.4V	13.0V

effect on the cross-domain voltages. The voltage overshoot at the receiver gate decreases by about 3%–13% compared with the reference depending on the configuration.

VII. CONCLUSION

The predictive CDM simulation methodology developed in this paper has been successfully demonstrated in a BiCMOS IC. The simulated CDM current waveforms perfectly match with actual measured CDM current discharge waveforms from calibration modules and real IC packages. Furthermore, the simulated cross-domain voltages compared with the measured breakdown voltages of the NMOST and the PMOST of the BiCMOS process in the CDM regime could explain the observed failure mechanism of the test case due to CDM stress. The impact of bond wires on cross-domain voltages has been studied as well.

The main limitations of this methodology are related to the simplification of the IC layout prior to electromagnetic simulations and the use of a TDR tool along with high-bandwidth 50-Ω-characteristic-impedance TDR probes. These TDR probes can hardly be used for all kind of IC packages due to their fixed pitch.

Some investigations are currently being done to use an electromagnetic 3-D solver for transient simulations of the IC packages. The purpose is to overcome the TDR probes limitation.

ACKNOWLEDGMENT

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